**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A computer implemented method in an instruction cache of a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle at an instruction cache unit, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;

responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit, wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction, ~~wherein~~ the incrementing ~~provides~~ providing a count of a number of times the instruction is executed; and

sending the bundle from the instruction cache unit to a functional unit for execution of the instruction.

2-5. (Canceled)

6. (Currently Amended) The computer implemented method of claim 1, wherein the counter is located in a shadow memory.

7-25. (Canceled)

26. (Currently Amended) The computer implemented method of claim 1, ~~further comprising using a spare field in~~ wherein the bundle [[to]] contains the indicator in a spare field of the bundle.

27. (Canceled)

28. (Canceled)

29. (Currently Amended) The computer implemented method of claim 1, further comprising:

responsive to a determination that the bundle contains the indicator, ~~beginning~~ incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

30. (Currently Amended) The computer implemented method of claim 29, wherein the bundle is a first bundle, the method further comprising:

receiving a second bundle at the instruction cache;

responsive to receiving the second bundle, determining whether a second instruction in the second bundle contains a second indicator; and

responsive to a determination that the second bundle contains the second indicator, ending the incrementing of the counter.

31. (Canceled)

32. (Currently Amended) A computer program product comprising:

a computer ~~readable~~ recordable medium having computer useable program code for monitoring execution of instructions, the computer program product comprising:

computer usable program code for receiving a bundle at an instruction cache unit, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;

computer usable program code for, responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

computer usable program code for, responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit, wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction, wherein the incrementing provides a count of a number of times the instruction is executed; and

computer usable program code for, sending the bundle from the instruction cache unit to a functional unit for execution of the instruction.

33. (Canceled)

34. (Previously Presented) The computer program product of claim 32, wherein the computer usable program code for incrementing the counter further comprises computer usable program code for incrementing the counter, wherein the counter is located in a shadow memory.

35. (Currently Amended) The computer program product of claim 32 further comprising ~~further comprising using a spare field in~~ wherein the bundle [[to]] contains the indicator in a spare field of the bundle.

36. (Canceled)

37. (Canceled)

38. (Currently Amended) The computer program product of claim 32, further comprising:

computer usable program code, responsive to a determination that the bundle contains the indicator, ~~for beginning~~ incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

39. (Currently Amended) The computer program product of claim 38 wherein the bundle is a first bundle, the computer program product further comprising:

computer usable program code for receiving a second bundle at the instruction cache unit;

computer usable program code, responsive to receiving the second bundle, for determining whether a second instruction in the second bundle contains a second indicator; and

computer usable program code, responsive to a determination that the second bundle contains the second indicator, for ending incrementing the counter.

40-48. (Canceled)

49. (New) A computer-implemented method of monitoring software performance in a data processing system, the computer-implemented method comprising:

detecting an indicator associated with one of an instruction and a memory location unit of a processor;

responsive to detecting the indicator, incrementing a counter in an instruction cache unit that is associated with the indicator; and

analyzing, in a performance monitor unit, a value of the counter to determine a performance of the data processing system.

50. (New) The computer-implemented method of claim 49, wherein responsive to the indicator being associated with an instruction, the incrementing occurs each time an instruction is executed.

51. (New) The computer-implemented method of claim 49, wherein responsive to the indicator being associated with a memory location unit, the incrementing occurs each time the memory location unit is accessed.

52. (New) The computer-implemented method of claim 49, further comprising:

generating an interrupt from an interrupt unit responsive to the value of the counter exceeding a threshold value.

53. (New) The computer-implemented method of claim 49, further comprising:

including a criteria for the counter; and

generating an interrupt from an interrupt unit responsive to meeting the criteria.